# Jashwanth Bamidi

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## Education

**University of Illinois Urbana-Champaign** — Champaign, IL
*Bachelor of Science in Computer Engineering* — *Expected Graduation: May 2028*
**GPA**: 3.8/4.00
**Relevant Coursework**: Electronic Circuits, Digital Signal Processing, Advanced Digital Projects Lab, FPGA Laboratory, Digital Logic Design, Advanced Digital Design, Computer Organization and Design, Computer Architecture, Computer Systems, Data Structures

## Experience

**Archer Aviation** — May 2026 – Aug 2026
*Electrical Engineering Intern* — *San Jose, CA*

- Owned a **2-layer Ethernet flow-control PCB** end to end in **Altium Designer**: multi-sheet **schematic capture**, **layout**, **Gerber/NC drill** outputs, BOM sourcing, in-house assembly, and **board bring-up**, replacing manual control on an inverter test stand.
- Designed the analog signal chain and power: a PWM-to-analog **RC filter** into an **LM358** 2x gain stage for a 0–10 V valve command, divided sensor feedback into the ADC, and **24 V** regulated to **5 V** and **3.3 V** rails.
- Root-caused a **0.9 ohm** 24 V-to-ground short to a copper clearance rule set in the wrong units and specified the re-spin.
- Validated the PCB's 0–10 V analog command and feedback paths using injected test voltages and ADC readback, then deployed **3 boards** across inverter test stands for remote cooling-flow control.
- Wrote embedded **C++** firmware for an **ATmega328P** interfacing with a **W5500** Ethernet controller, implementing **PID** control with anti-windup, **TCP** commands, and a 5 s communication fail-safe.
- Designed and wired a **1000 V** reliability stand supporting **3 inverter DUTs** concurrently with HV/LV power distribution, multiple **CAN-FD** gateways on a switched Ethernet network, a hardwired **E-STOP** and interlock chain, and an operator status tower light.
- Automated **SCPI** control of a 4-channel programmable supply over Ethernet, verifying every setpoint by readback before output enable, and collapsed a 4-step manual CAN-FD gateway setup into one **Python** script checked against reference configurations.
- Corrected an **AEC-Q101** accelerated reliability plan, fixing a Coffin-Manson acceleration factor from **12.7 to 7.7**, derived a **43-day** single-chamber thermal-cycling and humid-heat qualification schedule, and authored the controlled test documents.

**Eco Illini** — Aug 2025 – Present
*Power Distribution Unit Lead* — *Champaign, IL*

- Designed and laid out the vehicle's **4-layer Power Distribution Unit PCB** in **KiCad**, stepping a **36 V** battery bus down to **12 V** and **3.3 V** rails with buck converters and LDO regulators, owning schematic capture, component selection, and layout.
- Built in fusing, **reverse-polarity protection**, E-STOP integration, and temperature sensing, then assembled the outside-fabricated board in house and validated load regulation, transient response, thermal behavior, and in-vehicle integration.
- Held both rails under **50 mV** peak-to-peak ripple, verified in **LTspice** simulation and on the bench with an **oscilloscope**.
- Cut prototype iteration cycles **30%** year over year leading the PDU and **Joule Meter** PCB teams.
- Achieved under **1%** energy measurement error with register-level **STM32** firmware for an **INA228** on a 10 mΩ shunt, checked against a calibrated supply, and streamed real-time energy telemetry to powertrain subsystems over **CAN**, **SPI**, and **I2C**.

**Spatial Audio Research, UIUC** — Aug 2025 – Present
*Undergraduate Researcher – Advised by Prof. Yu-Lin Wei* — *Champaign, IL*

- Kept sound sources world-locked under live head motion with a real-time **binaural audio** pipeline fusing an **MPU6050 IMU** over I2C with Python **HRTF convolution** (SciPy FFT), using real-time **barycentric interpolation** in place of nearest-neighbor lookup.
- Improved perceived latency by training a **sequence model** on inertial and audio features to predict head pose **100 ms** ahead.

## Projects

**Hardware Guitar Auto-Tuner** | *Analog Circuit Design, Op-Amps, RLC Filters, Oscilloscope, Waveform Generator*

- Designed a fully **analog** guitar auto-tuner signal chain: a biased microphone front end with op-amp gain stages, **630/690 Hz RLC band-pass** discriminator paths with peak detectors and comparators around a 660 Hz target, and **H-bridge** closed-loop peg correction.
- Characterized each stage with a **waveform generator** and **oscilloscope**, and root-caused a comparator collapse during integration to a wiring short in the decision logic, restoring above/below pitch indication, after isolating circuit faults with injected test tones.

**FPGA Edge Detection Pipeline** | *SystemVerilog, FPGA Bring-Up, Sensor Interfaces, HDMI, CDC*

- Brought up a live **640x480 OV7670** camera-to-**HDMI/TMDS** FPGA pipeline, configuring the sensor over open-drain **SCCB/I2C** with ACK checking and reconstructing RGB565 pixels from its 8-bit parallel bus, with test patterns and status LEDs for bring-up.
- Stabilized video across 100 MHz system, 25 MHz PCLK, and 5x HDMI clocks with dual-clock framebuffering, **CDC** logic, and **XDC** constraints, streaming **Sobel edge detection** through rotating 640-pixel line buffers with sync delayed to match pipeline latency.

**VisionVest – Wearable Assistive Navigation** | *Embedded C++, ESP32-S3, BLE, PWM, Ultrasonic Sensors*

- Built an **ESP32-S3** haptic vest driving four 5 kHz **PWM** vibration motors and three ultrasonic rangefinders, commanded by **iPhone Core ML** perception over a **JSON BLE** protocol with type and range validation on every field and duplicate-packet rejection.
- Implemented nonblocking ultrasonic acquisition with five-sample filtering, 300 ms command expiry, and mode arbitration, plus a React Wi-Fi telemetry dashboard separating commanded from applied motor output and live sensor hazards for hardware debug.

**Pipelined RISC-V CPU Core** | *SystemVerilog, RTL Design, Vivado, FPGA*

- Designed a **5-stage pipelined RV32I CPU core** in SystemVerilog with a modular datapath and control partition, reaching **3.8x** throughput vs. a single-cycle baseline at near-**1 CPI** via forwarding, load-use hazard detection, and branch flush logic.
- Validated across **100+ directed and randomized tests** in **Vivado XSim** and closed timing on a RealDigital Blackboard FPGA.

**FPGA Order Book Engine** | *SystemVerilog, AXI4-Lite, MicroBlaze, Spartan-7*

- Built a **Spartan-7** order book engine chaining **Ethernet/IPv4/UDP** parsers, an ITCH-style decoder, and top-of-book RTL, integrated into a **MicroBlaze** SoC over **AXI4-Lite** at 100 MHz, 13k LUT, and 280 mW, with a packet-injection FIFO and valid/drop counters.

## Technical Skills

**PCB and Hardware Design**: Altium Designer, KiCad, Schematic Capture, PCB Layout, Power Tree Design, Buck and LDO Regulation, Component Selection, Protection Circuits, Footprints, LTspice, DFM, DRC, BOM, Gerber/NC Drill, Design Review
**Bring-Up and Test**: Board Bring-Up, Failure Analysis, Load/Transient/Thermal Testing, Reliability Testing, SCPI Automation, Oscilloscope, Multimeter, Bench Supply, Logic Analyzer, Waveform Generator, Root Cause Analysis, Soldering and Rework
**Embedded and Interfaces**: Bare-Metal C/C++, ATmega328P, STM32, ESP32, CAN/CAN-FD, Ethernet, SPI, I2C, UART, BLE
**Software and Digital**: Python, C, C++, MATLAB, SystemVerilog, Verilog, Vivado, Quartus, ModelSim, Git, Linux